CLAIMS

What is claimed is:

1. A method for forming a liquid crystal on silicon (LCOS) display spacer and groove in a multi-step etching process comprising the steps of:

providing a silicon substrate comprising a first overlying dielectric insulating layer and metal pixel electrodes;

forming a second dielectric insulating layer over the metal pixel electrodes;

forming a hardmask layer over the second dielectric insulating layer;

photolithographically patterning a resist layer formed over the hardmask layer and plasma etching the hardmask layer to form an etching mask for etching spacers in the second dielectric insulating layer;

carrying out a first plasma etching process to form spacers;

removing remaining resist layer portions and polymer etching residues over the process surface; and,

carrying out a second plasma etching process to etch grooves between metal pixel electrodes adjacent the spacers.

2. The method of claim 1, wherein the hardmask layer is selected from the group consisting of silicon nitride and silicon oxynitride.

3. The method of claim 1, wherein the hardmask layer comprises silicon nitride formed by a CVD process selected form the group consisting of LPCVD and PECVD.

4. The method of claim 1, wherein the first and second dielectric insulating layers comprise silicon dioxide (SiO_2).

5. The method of claim 1, wherein the first and second dielectric insulating layers comprise silicon dioxide (SiO_2) formed by a PECVD process.

6. The method of claim 1, further comprising at least one of an in-situ primarily oxygen containing plasma etch performed at least once during the second plasma etching process.

7. The method of claim 1, wherein the first and second plasma etching chemistries comprises plasma source gases selected from the group consisting of fluorocarbons, hydrofluorocarbons, and oxygen.

8. The method of claim 1, wherein a polymer passivation layer is formed over the process surface following the first plasma etching process.

9. The method of claim 1, wherein the step of removing is selected from the group consisting of a wet stripping and oxygen ashing.

10. The method of claim 1, wherein the spacers are formed to span pairs of metal pixel electrodes.

11. The method of claim 1, wherein the grooves are formed between metal pixel electrodes comprising the pairs of metal pixel electrodes and an adjacent metal pixel electrode.

12. The method of claim 1, wherein the grooves are formed to a depth extending below the metal pixel electrodes.

13. The method of claim 1, wherein the height of the spacers is from about 8,000 Angstroms to about 12,000 angstroms.

14. The method of claim 1, wherein the metal pixel electrodes comprise an aluminum-copper alloy.

15. A method for forming a liquid crystal on silicon (LCOS) display spacer and groove in a multi-step etching process comprising the steps of:

providing a silicon substrate comprising a first overlying silicon oxide layer and metal pixel electrodes;

forming a second silicon oxide layer over the metal pixel electrodes;

forming a hardmask layer comprising silicon nitride over the second silicon oxide layer;

photolithographically patterning a resist layer and performing a first plasma etch process to form a spacer spanning a first pair of metal pixel electrodes including forming a polymer passivation layer over the spacer sidewalls;

removing remaining resist layer portions and polymer passivation layer according to a wet etching process; and,

carrying out a second plasma etching process to etch a groove into the first silicon oxide layer between a metal pixel electrode formed adjacent the first pair of metal pixel electrodes and the first pair of metal pixel electrodes.

16. The method of claim 15, further comprising an in-situ primarily oxygen containing plasma etch performed at least once during the second plasma etching process.

17. The method of claim 15, wherein the silicon nitride hardmask layer is formed by a CVD process selected form the group consisting of LPCVD and PECVD.

18. The method of claim 15, wherein the first and second silicon oxide layers comprise silicon dioxide (SiO_2) formed by a PECVD process.

19. The method of claim 15, wherein the first and second plasma etching chemistries comprises plasma source gases selected from the group consisting of fluorocarbons, hydrofluorocarbons, and oxygen.

20. The method of claim 15, wherein the groove is formed to a depth extending below the metal pixel electrodes.

21. The method of claim 20, wherein the groove is formed to a depth of from about 4000 to about 8000 Angstroms.

22. The method of claim 15, wherein the height of the spacer is from about 8,000 Angstroms to about 12,000 angstroms.

23. The method of claim 15, wherein the metal pixel electrodes comprise a TiN barrier layer and an aluminum-copper alloy.

24. The method of claim 15, wherein the spacer is formed having sidewall inclined at an angle between about 65 degrees and about 75 degrees with respect to a horizontal plane in the substrate.